

1	2	3	4	5	6
Board Name Fabrication Document					
A					A
B					B
C					C
D					D
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	Comments:	Company: Company Name		Variant: Variant Name	
		Board Name: Board Name		Project Name: Project Name	
	Sheet Title: Board Name Assembly	File Name: KDT_Hierarchical.kicad_pcb	Designer: Designer Name	Date: 2024-01-25	Revision: 1.0
	Sheet Path:		Reviewer: Reviewer Name	Size: A4	Sheet: 1 of 1

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FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1)
- 2)

All dimensions are in millimeters unless otherwise specified.

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Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
	F.Paste				Paste Mask	GBR
	F.Silkscreen				Legend	GBR
	F.Mask			Solder Resist	Solder Mask	GBR
	Copper	L1 (Sig, PWR)	0.07mm (2oz)		Signal	GBR
	Prepreg		0.18mm	FR-4	Dielectric	
	Copper	L2 (GND)	0.035mm (1oz)		Internal Plane	GBR
	Core		0.4mm	FR-4	Dielectric	
	Copper	L3 (Sig, PWR)	0.035mm (1oz)		Signal	GBR
	Prepreg		0.18mm	FR-4	Dielectric	
	Copper	L4 (Sig, PWR)	0.035mm (1oz)		Signal	GBR
	Core		0.4mm	FR-4	Dielectric	
	Copper	L5 (GND)	0.035mm (1oz)		Internal Plane	GBR
	Prepreg		0.18mm	FR-4	Dielectric	
	Copper	L6 (Sig, PWR)	0.07mm (2oz)		Signal	GBR
	B.Mask			Solder Resist	Solder Mask	GBR
	B.Silkscreen				Legend	GBR
	B.Paste				Paste Mask	GBR
Total thickness: 1.62mm						
Note: external layer thicknesses are specified after plating.						

FABRICATION NOTES (CONT.)

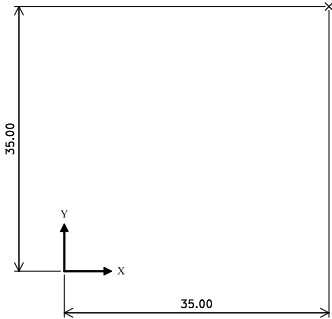
- 3) IMPEDANCE CONTROL REQUIRED. ?
Microstrip ???-Ohm Differential (L? ref. L?, L? ref. L?)
??mm width, ??mm spacing
- 4) CONFIRM TRACE WIDTHS AND SPACINGS.
- 5) DESIGN GEOMETRY MINIMUM FEATURE SIZES:
TRACE WIDTH ?? mm TRACE TO TRACE ?? mm
MIN. HOLE (plated) ?? mm MIN. HOLE (unplated) ?? mm
ANNULAR RING ?? mm COPPER TO HOLE ?? mm
COPPER TO EDGE ?? mm HOLE TO HOLE ?? mm

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TP??	??	??	??
TP??	??	??	??
TP??	??	??	??

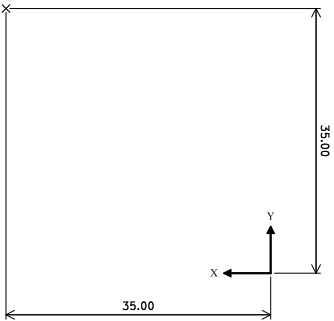


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TP??	??	??	??
TP??	??	??	??
TP??	??	??	??



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